## REMARKS

In the Office Action dated June 29, 2004, pending Claims 1-30 were examined and rejected. In response, Claims 1, 4, 5, 9, 15, 17, 18, 21, 23, 24 and 26 are amended, Claims 8, 16, 20, 22 and 26-30 are cancelled and no claims are added. Applicant reserves the right to prosecute the former claims in a divisional or continuation application. Applicant respectfully requests reconsideration of pending Claims 1-7, 9-15, 17-19, 21 and 23-25 in view of at least the following remarks.

### I. Claims Rejected Under 35 U.S.C. §102

The Examiner has rejected Claims 1-3, 10, 11, 16, 22, 26 and 27 under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 4,816,815 to Yoshiba. ("Yoshiba"). Applicant respectfully traverses this rejection.

Regarding Claim 1, Claim 1 is amended to recite the following claim features, which are neither taught nor suggested by either Yoshiba or the references of record:

> a first frame buffer divided into a plurality of regions;
>
> . . .; and
>
> a controller to simultaneously copy data within at least one region of the first frame buffer including updated data to both the second frame buffer and to the display monitor as the updated data within the region is needed to refresh the display monitor. (Emphasis added.)

Yoshiba describes refreshing of a CRT with updated display data with reference to FIGS. 8 and 14. As described within Yoshiba:

> after the display data in the region 314 has been fully updated, the CPU 20 transfers a start address SA associated with the region 314 to a start address latch 304a and an end address EA to an end address latch 304b. (*See*, col. 8, lines 26-30.)

As further described within Yoshiba:

> As the contents of the address counters 155 and 168 equal each with the start address SA of the specific region 314, the output 310 of the comparator 300a turns itself to high level and, due to the high level of the output 312 of the comparator 300b, turns the signal OBS1 to high level.
>
> The signal OBS1 now high level enables the display data buffer 164 and sets the data input/output buffer 122 of the VRAM 24 to a write mode. Then, the data stored in the region 314 of the VRAM 16 are sequentially read out and transferred to the CRT 10 to be displayed thereon, while being transferred to the VRAM 24 to be sequentially written in the region 320. (*See*, col. 8, line 60 - col. 9, line 4.)

As indicated by the cited passages above, CPU 20 as taught by Yoshiba, is responsible for transferring a start address SA and end address EA associated with updated data stored in VRAM 16. Conversely, Claim 1 recites a first frame buffer divided into a plurality of regions, such that when a region contains updated data, the entire region is simultaneously copied to both the second frame buffer and the display monitor as data within the region is needed to refresh the display monitor, as recited by amended Claim 1. Applicant respectfully submits that Yoshiba teaches away from the above-recited features of Claim 1, since Yoshiba specifically requires that:

> Only the data in the desired part 420 may be read out of the VRAM 16 and transferred to the CRT 10 while being written in an associated region of the VRAM 24. (*See*, col. 9, lines 46-49.)

As further described within Yoshiba:

> As seen from the foregoing description, addresses are compared also in the horizontal direction of the picture frame so that only the display data in the particular region 420 which the CPU 20 updated is read out of the VRAM 16 and displayed on the CRT 10 and, at the same time, its copy is reproduced in the VRAM 24. (*See*, col. 10, lines 5-11.) (Emphasis added.)

Applicant respectfully submits that the teachings of Yoshiba are strictly directed to copying only the display data in the region which has been updated by CPU 20 so that:

> . . . access by the CPU 20 to the VRAM 16 is inhibited only for a period wherein display data are sequentially read out of the region 314 of the VRAM 16 and transferred to the CRT 10. This offers the CPU a longer period of time within which it can make access to the VRAM 16 than in the case of the first embodiment. (*See*, col. 9, lines 36-42.) (Emphasis added.)

In other words, Yoshiba describes two embodiments for handling of updated data:

> . . . the first embodiment would transfer one frame of display data from the VRAM 16 to the CRT 10 and VRAM 24 despite the partial change of the display data, that is, it could develop a copy of one frame of display data in the VRAM 24 despite the partial change of the display data. In contrast, in accordance with the second embodiment, only the region 314 updated anew is transferred. (*See*, col. 8, lines 1-9.) (Emphasis added.)

Accordingly, Applicant respectfully submits that Yoshiba provides no teachings or suggestions with regards to dividing a first frame buffer into a plurality of regions and simultaneously copying at least one region, including updated data to both the second frame buffer and the display as recited by Claim 1. Accordingly, Applicant respectfully submits that the Examiner is prohibited from establishing a *prima facie* case of anticipation of Claim 1, as amended, since the Yoshiba reference fails to teach or suggest each of the recited features of Claim 1, as amended.

Accordingly, Claim 1, as amended, is patentable over Yoshiba, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claim 1.

Regarding Claims 2 and 3, Claims 2 and 3 depend from Claim 1, and therefore include the patentable claim features of Claim 1, as described above. Accordingly, Claims 2 and 3, based on their dependency from Claim 1, are also patentable over Yoshiba, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §102(b) rejection of Claims 2 and 3.

## II. Claims Rejected Under 35 U.S.C. §103

The Examiner has rejected Claims 4-6, 12-15, 17-19, 21, 23-25 and 28-30 under 35 U.S.C. §103(a) as being unpatentable over Yoshiba as applied to Claim 3 in view of U.S. Patent No. 5,757,364 to Ozawa et al. ("Ozawa"). Applicant respectfully traverses this rejection.

To establish a *prima facie* case of obviousness, the following criteria must be met: (1) there must be some suggestion or motivation to modify the reference or combine the reference teachings, (2) there must be a reasonable expectation of success, and (3) the prior art references must teach or suggest all the claim limitations. (MPEP §2142)

Regarding the Examiner's citing of Ozawa, Applicant respectfully submits that Ozawa fails to rectify the deficiencies attributed to Yoshiba for failing to teach a first frame buffer divided into a plurality of regions and the simultaneous copying of data within at least one region of the first frame buffer, including updated data to both the second frame buffer and the display monitor as data within the region is needed to refresh the display monitor.

The Examiner cites Ozawa to teach a detector for detecting when an update is made to the data in the frame buffer and a decoder for decoding the location of the updated data. In fact, Applicant respectfully submits that one skilled in the art would not modify Yoshiba in view of Ozawa to teach a detector for detecting when an update is made to the data in the frame buffer and a decoder for decoding the location of the updated data since CPU 20, as taught by Yoshiba, already provides such information in the form of start address SA and end address EA. (*See*, col. 8, lines 26-30.)

Accordingly, Applicant respectfully submits that the Examiner is prohibited from establishing a *prima facie* case of obviousness of amended Claim 1 since the combination of Yoshiba in view of Ozawa, fails to teach or suggest the recited features of a first frame buffer divided into a plurality of regions and the simultaneous copying of data within at least one region of the first frame buffer including updated data to both the second frame buffer and the display monitor as data within the region as needed to refresh the display monitor. Accordingly, Claim 1,

as amended, is patentable over the combination of Yoshiba in view of Ozawa, as well as the references of record.

Regarding Claims 4-6, Claims 4-6 depend from Claim 1, and therefore include the patentable claim features of Claim 1, as described above. Accordingly, Claims 4-6, based on their dependency from Claim 1, are also patentable over the combination of Yoshiba in view of Ozawa, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 4-6.

Regarding Claim 15, Claim 15 is amended to recite the following claim features, which are neither taught nor suggested by either Yoshiba, Ozawa or the references of record:

> identifying, within a first frame buffer memory divided into a plurality of regions, at least one region including updated data; . . .
>
> simultaneously copying data within the identified region of the first frame buffer memory to both the second frame buffer memory and to a display monitor as the data within the region is needed to refresh the display monitor.

As indicated above with reference to Claim 1, Yoshiba is devoid of any teachings with regards to a first frame buffer, which is divided into a plurality of regions or the identification of at least one region including updated data. Applicant submits that Yoshiba is devoid of such teachings since CPU 20 of Yoshiba updates a start address SA and end address EA of updated data. Likewise, Yoshiba is devoid of any teachings with regards to the simultaneous copying of data within the identified region of the first frame buffer to both the second frame buffer and to a display monitor as data within the regions needed to refresh the display monitor.

Applicant respectfully submits that Yoshiba teaches away from such recited claim features since Yoshiba is strictly limited to copying only the display data which the CPU 20 updated in order to reduce the amount of time in which access to VRAM 16 is inhibited. (*See*, col. 8, lines 1-9.) Furthermore, Applicant respectfully submits that the Examiner's citing of Ozawa fails to rectify the above-described deficiencies of Yoshiba in failing to teach each of the recited claim features of Claim 15, as amended.

Accordingly, Applicant respectfully submits that the Examiner is prohibited from establishing a *prima facie* case of obviousness of Claim 15, as amended, in view of the combination of Yoshiba and Ozawa, since the combination fails to teach each of the recited claim features of Claim 15, as amended. Accordingly, Claim 15, as amended, is patentable over the combination of Yoshiba in view of Ozawa, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 15 and 21.

Regarding Claims 17-19, Claims 17-19 depend from Claim 15, and therefore include the patentable claim features of Claim 15, as described above. Accordingly, Claims 17-19, based on their dependency from Claim 15, are also patentable over the combination of Yoshiba in view of

Ozawa, as well as the references of record. Consequently, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 17-19.

Regarding Claims 23-25, Claims 23-25 depend from Claim 21, and therefore include the patentable claim features of Claim 21, as described above. Accordingly, Claims 23-25, based on their dependency from Claim 21, are also patentable over the combination of Yoshiba in view of Ozawa, as well as the references of record. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 23-25.

The Examiner has rejected Claims 7-9 and 20 under 35 U.S.C. §103(a) as being unpatentable over Yoshiba, as applied to Claim 1, in view of U.S. Patent No. 4,816,815 to Hsu ("Hsu"). Applicant respectfully traverses this rejection.

Regarding Claims 7-8, Claims 7-8 depend from Claim 1, and therefore include the patentable claim features of Claim 1, as amended. Regarding the Examiner's citing of Hsu, Applicant respectfully submits that Hsu fails to rectify the above-described deficiencies of Yoshiba in failing to teach or suggest a first frame buffer divided into a plurality of regions and a controller to simultaneously copy data within at least one region of the first frame buffer, including updated data to both the second frame buffer and the display monitor as data within the regions needed to refresh the display monitor.

Accordingly, Applicant respectfully submits that Claim 1, as amended, is patentable over the combination of Yoshiba in view of Hsu. Likewise, Claims 7-8, based on their dependency from Claim 1, are also patentable over the combination of Yoshiba in view of Hsu. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claims 7-8.

Regarding Claim 9, Claim 9 is amended to recite the following claim features, which are neither taught nor suggested by either Yoshiba, Hsu or the references of record, whether viewed in combination or independently:

> a unified memory including a main memory and a primary frame buffer memory divided into a plurality of regions;
>
> . . ., and
>
> a controller to simultaneously copy pixel data within at least one region of the primary frame buffer memory including updated data to both the secondary frame buffer memory and to the display monitor as the pixel data within the region is needed to refresh the display monitor.

The Examiner cites Hsu to teach the first frame buffer as part of a unified memory architecture. However, Applicant respectfully submits that Hsu fails to rectify the above-described deficiencies of Yoshiba in failing to teach or suggest a first frame buffer divided into a plurality of regions and a controller to simultaneously copy data within at least one region of the first frame

buffer, including updated data to both the second frame buffer and the display monitor as data within the regions needed to refresh the display monitor.

Accordingly, Applicant respectfully submits that Claim 9, as amended, is patentable over the combination of Yoshiba in view of Hsu. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the §103(a) rejection of Claim 9.

## CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR, & ZAFMAN LLP

Dated: August 24 2004

By: _____
Joseph Lutz, Reg. No. 43,765

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, California 90025
(310) 207-3800

**CERTIFICATE OF MAILING**
I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. 1450, Alexandria, VA 22313-1450 on August 24, 2004.

Marilyn Bass August 24, 2004